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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KROFCHECK, MICHAEL C	
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,555	CHOI ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,18-20,24-27,39-42,44,46,49-57,65-78 and 80-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *92 and 94* is/are allowed.

6)☒ Claim(s) *1-14,18-20,24-27,39-42,44,46,49-57,65-78,80,83-91,93 and 95* is/are rejected.

7)☐ Claim(s) *81 and 82* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/15/2006, 12/18/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the RCE filed on 12/18/2006.

2. Claims 1, 5, 8, 11, 18, 24, 49, 53, 57, 65-66, 68-69, 72-73, 76, 78 have been amended.

3. Claims 15-17, 21-23, 28-38, 43, 45, 47-48, 58-64, 79 are cancelled.

4. Claims 80-95 have been added and examined.

5. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

Claim Objections

6. Claims 91, 93, and 95 are objected under 37 CFR 1.75 as being substantial duplicates of each other. All three claims are dependent on claim 90, it appears that they were intended to depend on claims 90, 92, and 94. However, if claims 93 and 95 are dependent on claims 92 and 94, they would be rejected under 112 second paragraph, since in claims 92 and 94 there is no mention of the quantities J and F which are qualified in claims 93 and 95.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 89, 91, 93, 95 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no explicit reference in the specification stating that the number of address pins cannot be a multiple of the number of bit word being received. The examiner invites the applicant to point out the exact location that this is stated, in the specification, if there is support for the limitation.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 90-91, 93, 95 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 90 recites the limitation "the fully-received F-bit word" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 1-4, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeMone et al., US patent 6266750, Schaefer, US patent 5666321, and Fujima et al., US patent 6392951.

15. With respect to claim 1, DeMone teaches of a method of operating a memory device, comprising: receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals (column 3, lines 44-51; column 4, lines 29-33; the 40-bit command packet is a word),

wherein receiving the F-bit word comprises: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; column 4, lines 29-33; where F is 40 bits),

wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of the set of command and address signals (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). G is 10 bits, which is less than 40. It is abundantly

clear to one of ordinary skill in the art that the command packet can be considered a word since the packet in its entirety is needed to access the memory); and

receiving a second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5),

wherein the second portion of the F-bit word comprises H-bits, wherein the H-bit portion comprises a second subset of the set of command and address signals (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). H is 10 bits),

performing a memory command in response to the received F-bit word (fig. 5a, column 5, lines 10-32).

DeMone fails to explicitly teach of wherein H is F-G; and wherein the set of command and address signals consists of an active command, bank address signals, and row address signals.

However, Schaefer teaches of wherein H is F-G (column 1, lines 28-32; where the memory address is broken down into two parts. Thus the size of the second part is equal to the size of the entire address minus the size of the first part).

Fujima teaches of wherein the set of command and address signals consists of an active command, bank address signals, and row address signals (column 5, lines 35-45).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone and Schaefer at the time of the invention to use two (or any other number)

10-bit groups to make the command packet of DeMone as taught in Schaefer. Their motivation would have been to enable the invention of DeMone to operate with different memories which require different sized command words/packets.

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Schaefer, and Fujima at the time of the invention to use the bank activate command of Fujima in the combination of DeMone and Schaefer. Their motivation would have been to provide compatibility with other current memory systems as it is known in the art (Fujima, column 5, lines 19-45).

16. With respect to claim 2, DeMone teaches of wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device (fig. 1-2; column 3, lines 20-42; the memory device is a SLDRAM which is a type of DRAM).

17. With respect to claim 3, DeMone teaches of sending the first portion of the F-bit word substantially simultaneous with sending the first edge of the clock signal by an external controller; and sending the second portion of the F-bit word substantially simultaneous with sending the second edge of the clock signal by the external controller (fig. 1, 2a, 3b; column 3, lines 22-30; column 3, line 61-column 4, line 5; where the command module sends the command/address signals and the clock signal).

18. With respect to claim 4, DeMone teaches of in sending, the external controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor (fig. 1; column 3, lines

22-30; as the command module, implemented by a memory controller, controls a type of DRAM, it must be a DRAM controller).

19. With respect to claim 39, DeMone teaches of wherein the integrated circuit memory device is a volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM, which is a type of volatile memory).

20. Claims 5-14, 40-42, 55-56, 74-75, 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeMone, Schaefer, Fujima, and Ohshima et al., US patent application publication 2001/0006483.

21. With respect to claim 5, DeMone teaches of a method of operating a memory device, comprising: receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals (column 3, lines 44-51; column 4, lines 29-33),

wherein receiving the F-bit word comprises: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A0);

wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). G is 10 bits, which is less than 40. It is abundantly clear to one of ordinary skill in the art that the command packet can be considered a word since the packet in its entirety is needed to access the memory);

receiving a second portion of the F-bit word (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A2),

wherein the second portion of the F-bit word comprises H-bits (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). H is 10 bits, which is less than 40); and

performing a memory command in response to the received F-bit word (fig. 5a, column 5, lines 10-32).

DeMone Fails to explicitly teach of wherein wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals; wherein the H-bit portion comprises a second subset of the set of address signals; wherein H is F-G; wherein the set of command and address signals consists of an dacitave command, bank address signals, and row address signals.

However, Ohshima teaches of wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals (fig. 17; paragraph 0084; where the read command (command signals) and the upper address (1st part of the address) is received on the rising edge of the 1st clock cycle),

wherein the H-bit portion comprises a second subset of the set of address signals (fig. 17; paragraph 0084; where the lower address (2nd part of the address) is received on the rising edge of the 2nd clock cycle),

Schaefer teaches of wherein H is F-G (column 1, lines 28-32; where the memory address is broken down into two parts. Thus the size of the second part is equal to the size of the entire address minus the size of the first part).

Fujima teaches of wherein the set of command and address signals consists of an active command, bank address signals, and row address signals (column 5, lines 35-45).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to include the command signals and part of the address with the first portion and output the address with the second portion in DeMone as taught in Ohshima. Their motivation would have been to enhance the memory cell access speed without degrading the random access time (Ohshima, paragraph 0085).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Ohshima, and Schaefer at the time of the invention to use two (or any other number) 10-bit groups to make the command packet of the combination of DeMone and Ohshima as taught in Schaefer. Their motivation would have been to enable the combination of DeMone and Ohshima to operate with newer and older memories which require different sized command words/packets.

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Ohshima, Schaefer, and Fujima at the time of the invention to use the bank activate command of Fujima in the combination of DeMone and Schaefer. Their motivation would have been to provide compatibility with other current memory systems as it is known in the art (Fujima, column 5, lines 19-45).

22. With respect to claim 8, DeMone teaches of a method of operating a memory device, comprising: receiving an F-bit word, wherein F is a positive integer, wherein the

F-bit word comprises a set of command and address signals (column 3, lines 44-51; column 4, lines 29-33),

wherein receiving the F-bit word comprises: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A0);

wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of a set of command and address signals (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). G is 10 bits, which is less than 40. It is abundantly clear to one of ordinary skill in the art that the command packet can be considered a word since the packet in its entirety is needed to access the memory);

receiving a second portion of the F-bit word (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A2),

wherein the second portion of the F-bit word comprises H-bits, wherein the H-bit portion comprises a second subset of the set of command and address signals (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). H is 10 bits, which is less than 40); and

performing a memory command in response to the received F-bit word (fig. 5a, column 5, lines 10-32).

Ohshima teaches of wherein the second portion of the F-bit word is received substantially simultaneous with receiving a first edge of a second cycle of a clock signal (fig. 17; paragraph 0084).

Schaefer teaches of wherein H is F-G (column 1, lines 28-32; where the memory address is broken down into two parts. Thus the size of the second part is equal to the size of the entire address minus the size of the first part).

Fujima teaches of wherein the set of command and address signals consists of an active command, bank address signals, and row address signals (column 5, lines 35-45).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to output the second portion based on the rising edge of the next clock cycle in DeMone as taught in Ohshima. Their motivation would have been to allow a wider range of memory types to be used, with the same supporting circuitry lowering the cost.

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Ohshima, and Schaefer at the time of the invention to use two (or any other number) 10-bit groups to make the command packet of the combination of DeMone and Ohshima as taught in Schaefer. Their motivation would have been to enable the combination of DeMone and Ohshima to operate with newer and older memories which require different sized command words/packets.

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Ohshima, Schaefer, and Fujima at the time of the invention to use the bank activate command of Fujima in the combination of DeMone and Schaefer. Their motivation would have been to provide compatibility with other current memory systems as it is known in the art (Fujima, column 5, lines 19-45).

23. With respect to claim 11, DeMone teaches of a method of operating a memory device, comprising: receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals (column 3, lines 44-51; column 4, lines 29-33),

wherein receiving the F-bit word comprises: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A0);

wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). G is 10 bits, which is less than 40. It is abundantly clear to one of ordinary skill in the art that the command packet can be considered a word since the packet in its entirety is needed to access the memory);

receiving a second portion of the F-bit word (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A2),

wherein the second portion of the F-bit word comprises H-bits (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). H is 10 bits, which is less than 40); and

performing a memory command in response to the received F-bit word (fig. 5a, column 5, lines 10-32).

Ohshima teaches of wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals (fig. 17; paragraph 0084; where the

read command (command signals) and the upper address (1st part of the address) is received on the rising edge of the 1st clock cycle),

wherein the H-bit portion comprises a second subset of the set of address signals (fig. 17; paragraph 0084; where the lower address (2nd part of the address) is received on the rising edge of the 2nd clock cycle),

wherein the second portion of the F-bit word is received substantially simultaneous with receiving a first edge of a second cycle of a clock signal (fig. 17; paragraph 0084; where the lower address (2nd part of the address) is received on the rising edge of the 2nd clock cycle).

Schaefer teaches of wherein H is F-G (column 1, lines 28-32; where the memory address is broken down into two parts. Thus the size of the second part is equal to the size of the entire address minus the size of the first part).

Fujima teaches of wherein the set of command and address signals consists of an active command, bank address signals, and row address signals (column 5, lines 35-45).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to include the command signals and part of the address with the first portion and output the address with the second portion in DeMone as taught in Ohshima. Their motivation would have been to enhance the memory cell access speed without degrading the random access time (Ohshima, paragraph 0085).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to output the second portion based on the rising edge of the next clock cycle in DeMone as taught in Ohshima. Their motivation would have been to allow a wider range of memory types to be used, with the same supporting circuitry lowering the cost.

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Ohshima, and Schaefer at the time of the invention to use two (or any other number) 10-bit groups to make the command packet of the combination of DeMone and Ohshima as taught in Schaefer. Their motivation would have been to enable the combination of DeMone and Ohshima to operate with newer and older memories which require different sized command words/packets.

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Ohshima, Schaefer, and Fujima at the time of the invention to use the bank activate command of Fujima in the combination of DeMone and Schaefer. Their motivation would have been to provide compatibility with other current memory systems as it is known in the art (Fujima, column 5, lines 19-45).

24. With respect to claims 9 and 12, DeMone teaches of wherein, in receiving the second portion of the F-bit word, the second cycle is substantially subsequent to the first cycle (fig. 3b; column 3, line 61-column 4, line 5).

25. With respect to claims 6, 10, and 14, DeMone teaches of wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, a non-volatile memory device, a static random access memory

(SRAM) device, and a static memory device (fig. 1-2; column 3, lines 20-42; the memory device is a SLDRAM which is a type of DRAM).

26. With respect to claim 7, DeMone teaches of wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

27. With respect to claim 13, DeMone teaches of wherein a clock signal comprises a first and second edge, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

28. With respect to claims 40-42, DeMone teaches of wherein the integrated circuit memory device is a volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM, which is a type of volatile memory).

29. Claims 18-20, 24-27, 44, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeMone, Fujima, and Ohshima et al., US patent application publication 2001/0006483.

30. With respect to claim 18, the combination of DeMone, Fujima, and Ohshima teach of all the limitations of claim 18 cited above with respect to claim 8.

Additionally, DeMone inherently discloses multiple command and address pins to receive the first and second portions of the F-bit word (fig. 1; column 3, lines 20-30; as the SLDRAM is an IC (integrated circuit), there must be I/O pins connecting to the command link to enable the signals to be received from the command module as described. As there are 10 command/address lines, there must be 10 pins, which allow for the signals to be transferred from the memory chip; without the pins, the memory would not be connected to the CA[0:9] bus).

31. With respect to claim 24, the combination of DeMone, Fujima, and Ohshima teach of all the limitations of claim 24 which are cited above with respect to claims 18 and 8.

DeMone also teaches of a memory circuit comprising: one or more integrated circuit memory devices operable for sending and receiving signals (fig. 1; column 3, lines 20-30; where the SLDRAMs are individual ICs (integrated circuits) connected to a command module)

32. With respect to claims 19 and 27, DeMone teaches of wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device (fig. 1-2; column 3, lines 20-42; the memory device is a SLDRAM which is a type of DRAM).

33. With respect to claims 20, and 26, DeMone teaches of wherein a clock signal comprises a first and second edge, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the

rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

34. With respect to claim 25, DeMone teaches of wherein, in receiving the second portion of the F-bit word, the second cycle is substantially subsequent to the first cycle (fig. 3b; column 3, line 61-column 4, line 5).

35. With respect to claims 44 and 46, DeMone teaches of wherein the integrated circuit memory device is a volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM, which is a type of volatile memory).

36. Claims 49-52, 54, 65-71, 73, 78, 80, 83-91, 93, 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeMone, Schaefer, Fujima, and Kim, US patent application publication 2003/01213319.

37. With respect to claim 49, DeMone teaches of receiving an F-bit word using J command and address pins of a programmable memory device, wherein F and J are positive integers, wherein J is less than F, wherein the F-bit word comprises a set of command and address signals (fig. 1; column 3, lines 44-51; column 4, lines 29-33; the 40-bit command packet is a word, F is 40 and J is 10 as the CA[0:9] bus has a 10-bit capacity and must have 10 pins going into the SLDRAM module), comprising:

receiving a first portion of the F-bit word at a first time using G command and address pins, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein G is less than or equal to J (fig. 3b; column 4, lines 29-33; where

the 10-bits parts are combined to form a 40-bit command packet (word). G is 10 bits, which is less than 40 bits, which is also equal to the 10 pins into the module);

receiving a second portion of the F-bit word at a second time, wherein the second portion of the F-bit word comprises H-bits, wherein H is less than or equal to J (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). H is 10 bits, which is less than 40 and equal to the 10 pins); and

performing a memory command in response to the fully-received F-bit word (fig. 5a, column 5, lines 10-32).

Schaefer teaches of wherein H is F-G (column 1, lines 28-32; where the memory address is broken down into two parts. Thus the size of the second part is equal to the size of the entire address minus the size of the first part).

Fujima teaches of wherein the set of command and address signals consists of an active command, bank address signals, and row address signals (column 5, lines 35-45).

Demone fails to explicitly teach of wherein the first portion of the F-bit word consists of a set of command signals and a first subset of address signals, wherein the set of command signals includes a CS signal, a RAS signal, a CAS signal and a WE signal, wherein receiving the set of command signals includes using a set of command pins wherein the set of command pins include a CS pin, a RAS pin, a CAS pin, and a WE pin, wherein receiving the first subset of address signals includes using a set of

address pins and wherein the set of address pins include G-4 pins; and wherein the second portion of the F-bit word consists of a second subset of address signals.

However, Kim teaches of wherein the first portion of the F-bit word consists of a set of command signals and a first subset of address signals, wherein the set of command signals includes a CS signal, a RAS signal, a CAS signal and a WE signal, wherein receiving the set of command signals includes using a set of command pins wherein the set of command pins include a CS pin, a RAS pin, a CAS pin, and a WE pin (fig. 2; paragraph 0023-0024),

wherein the second portion of the F-bit word consists of a second subset of address signals (fig. 2; paragraph 0023-0024).

The combination of DeMone, Schaefer, Fujima, and Kim teaches of wherein receiving the first subset of address signals includes using a set of address pins and wherein the set of address pins include G-4 pins (it is abundantly clear to one of ordinary skill in the art that the address pins used are equal to G minus 4 since the total number of pins used is G and there are four command bit/pins being used)

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone and Schaefer at the time of the invention to use two (or any other number) 10-bit groups to make the command packet of DeMone as taught in Schaefer. Their motivation would have been to enable the invention of DeMone to operate with different memories which require different sized command words/packets.

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Schaefer, Fujima, and Kim at the time of the invention to incorporate the

signal and pin layout of Kim in the combination of DeMone, Schaefer, and Fujima. Their motivation would have been to reduce the number of pins (Kim, paragraph 0012).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Schaefer, and Fujima at the time of the invention to use the bank activate command of Fujima in the combination of DeMone and Schaefer. Their motivation would have been to provide compatibility with other current memory systems as it is known in the art (Fujima, column 5, lines 19-45).

38. With respect to claims 50-52, DeMone teaches of wherein a first time includes at or substantially simultaneously with receiving a first rising edge of a first clock cycle of a clock signal (fig. 3b; where A0 is received on the rising edge of a first period of the clock (CCLK)).

39. With respect to claim 54, DeMone teaches of wherein a second time includes at or substantially simultaneously with receiving a second edge of a clock signal (fig. 3b; where A1 is received on a second edge of the clock signal (CCLK)).

40. With respect to claim 65, DeMone teaches of wherein a programmable memory device includes a device selected from the group consisting of a DRAM device, a SRAM device, a static memory device, a flash memory device, and a non-volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM).

41. With respect to claim 66, DeMone teaches of wherein a programmable memory device includes a volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM, which is a type of volatile memory).

42. With respect to claim 67, DeMone teaches of sending the first portion of the F-bit word with a controller at a first time; and sending the second portion of the F-bit word with a controller at a second time (fig. 1, 2a, 3b; column 3, lines 22-30; column 3, line 61-column 4, line 5; where the command module sends the command/address signals and the clock signal).

43. With respect to claim 68, DeMone teaches of wherein a controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor (fig. 1; column 3, lines 22-30; as the command module, implemented by a memory controller, controls a type of DRAM, it must be a DRAM controller).

44. With respect to claims 69-71 and 73, DeMone teaches of the limitations as cited above with respect to claims 50-52 and 54, respectively.

45. With respect to claim 53 and 72, DeMone teaches of wherein the first edge is a falling edge of a clock signal (fig. 3b; it is abundantly clear to one of ordinary skill in the art to time shift a process by a half a clock cycle forwards or backwards to suit the overall system timing).

46. With respect to claim 78, the combination of DeMone, Schaefer, Fujima, and Kim teaches of wherein the programmable memory device consists of J command and address pins (it is abundantly clear to one of ordinary skill in the art that since the packets on the CA bus are 10 bits, that there are 10 pins; DeMone column 4, lines 29-35).

47. With respect to claim 80, Fujima teaches of wherein the set of address signals comprises bank address signals BA0-BA2 (fig. 10; column 5, lines 35-45; since there are 16 banks there must be 4-bit addresses).

Kim teaches of wherein the set of address signals comprises row address signals A0-A11 (fig. 2; where there address signal is a 14-bit signal).

48. With respect to claim 83, Kim teaches of wherein receiving the second subset of address signals includes using at least one of the set of address pins (fig. 2, paragraph 23-24).

49. With respect to claim 84, Kim teaches of wherein receiving the second subset of address signals includes using at least one command pin and at least one address pin (fig. 2, paragraph 23-24);

50. With respect to claim 85, Kim teaches of wherein the at least one command pin and the at least one address pin include using H command and address pins, wherein H is greater than G-4 (fig. 2, paragraph 23-24).

51. With respect to claim 86, Kim teaches of wherein the at least one command pin includes the RAS pin (fig. 2, paragraph 23-24).

52. With respect to claim 87, Kim teaches of wherein the at least one command pin includes the CAS pin (fig. 2, paragraph 23-24).

53. With respect to claim 88, Kim teaches of wherein the at least one command pin includes the WE pin (fig. 2, paragraph 23-24).

54. With respect to claim 89, Kim teaches of wherein J is not a multiple of F (fig. 2; where there are 14 pins (J) and the received word is 19 bits (F)).

55. With respect to claim 90, the combination of DeMone, Schaefer, Fujima, and Kim teaches of the limitations cited above with respect to claim 49.

Kim also teaches of wherein the second portion of the set of command and address signals consists of a second subset of address signals, and wherein receiving the second subset of address signals includes using at least one command pin and at least one address pin (fig. 2; paragraph 23-34).

56. With respect to claims 91, 93, 95, Kim teaches of the limitations cited above with respect to claim 89.

57. Claims 55-57, 74-77 rejected under 35 U.S.C. 103(a) as being unpatentable over DeMone, Schaefer, Fujima, and Kim as applied to claims 54, 73, 49 above, and further in view of Ohshima.

58. With respect to claims 55-56 Ohshima teaches of wherein the second edge of a clock signal includes a first rising edge of a second cycle of the clock signal (fig. 17; where the lower address (LA) is received on the rising edge of the second clock period).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Schaefer, Fujima, Kim and Ohshima at the time of the invention to output the second portion based on the rising edge of the next clock cycle in the combination of DeMone, Schaefer, Fujima, and Kim as taught in Ohshima. Their motivation would have been to allow a wider range of memory types to be used, with the same supporting circuitry lowering the cost.

59. With respect to claims 74-75, Ohshima teaches of the limitations as cited above with respect to claims 55-56.

60. With respect to claims 57 and 76, DeMone teaches of wherein the second edge is a falling edge of the clock signal (fig. 3b).

61. With respect to claim 77, Ohshima teaches of wherein H and G are not equal to each other (fig. 17; paragraph 0084, as the G-bit section includes the command and the upper address, and the H-bit section includes just the lower address, it is abundantly clear to one of ordinary skill in the art that H does not equal G, since it is clear that the upper and lower address portions are the same size).

Allowable Subject Matter

62. Claims 81, 82 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

63. Claims 92 and 94 are allowed.

64. The following is a statement of reasons for the indication of allowable subject matter:

a. The primary reason for allowance of claims 92, and 94 is the occurrence of the specific command signal values in combination with the other recited limitations.

Response to Arguments

65. Applicant's arguments with respect to independent claims 1, 5, 8, 11, 18, 24, and 49 have been considered but are moot in view of the new ground(s) of rejection.

66. Applicant's arguments filed on 11/17/2006 have been fully considered but they are not persuasive.

67. In response to applicant's argument that DeMone and Schaefer don't teach of H=F-G since the address portions of Schaefer are different than those in the claim limitations, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In the combination of DeMone and Schaefer, it is not the literal combination of the addresses portions, but the concept of the address being in two portions that is taken from Schaefer.

Conclusion

68. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

69. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

70. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

71. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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